REMARKS

(1) 35 USC 112 Rejection: (Claim 1, 13 & 17)

Please see the amended claims 1, 13 and 17. Withdrawal of the rejection is respectfully requested.

(3) 35 USC 103(a) Rejections (Claims 1-6, 13 and 17)

In section 3 of the office action, the examiner noted that:

> "Claims 1-6, 13 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ichimori et al. (US publication 2002/0036320) in combination with Vinal (US patent 5151759) and Houston (US publication 2002/0180069)."

Ichimori describes fabrication of an SOI thin film device comprising a fully salicided source/drain region, said salicided region further comprising a <111> silicon plane. The emphasis is to reduce the source/drain resistance and reduce junction leakages. No doping information or device operation is provided. This device falls under the prior art described by the Applicant in Fig-3 (page 6, line 13 – page 7, line 9).

Vinal describes a very specific "Fermi Threshold" SOI FET which is substantially independent of device dimensions. This "depletion type" device is constructed on sufficiently thick SOI film for a bulk region beneath the channel region not to be fully depleted. A generic non SOI depletion MOSFET was described by the Applicant under prior art in Fig-1 (page 5, lines 15-21).

Houston describes a DRAM comprising a pass-gate transistor wherein the gate material (thus gate work function) is varied to achieve a high Vt SOI device. No detailed doping information or device operation is provided. These devices also fall under the prior art described by the Applicant in Fig-3.

In contrast, the Applicant describes a new Gated-FET design, optimization, fabrication and operation. The new device is comprised of: forming a substantially rectangular channel region (not a bulk region) in said semiconductor thin film layer, said channel region lightly doped to form a resistive channel, wherein the height of the channel region comprising the entire thin film thickness (single dopant region). Above listed prior art individually or collectively do not show such a device. A detailed description is provided below.

(3.1) Claims 1, 13 & 17 rejection:

In section 3 of the office action, the examiner noted that:

> "Ichimori et al. fail to teach doping the channel region and optimizing the thin film layer, gate insulator, and gate material by providing the gate region with a first voltage level that modulates channel resistance to a substantially non-conductive state by fully depleting majority carriers from said channel region; and a second voltage level that modulates said channel resistance to a substantially conductive state by at least partially accumulating majority carriers near a surface of the gate insulator layer,
> Vinal teaches a method of fabricating a Gated-FET device comprised of doping the channel region 15 and optimizing the thin film layer, gate insulator, and gate material by providing the gate region with a first voltage level that modulates channel resistance to a substantially non-conductive state by fully depleting majority carriers from said channel region 15 and a second voltage level that modulates said channel resistance to a substantially conductive state by at least partially accumulating majority carriers in the channel region 15. See fig. 23 & col. 36, lines 56-61 and Figs. 24-25 and col. 36, line 65 to col. 37, line 10.
> It would have been obvious to one of ordinary skill in the art of making semiconductor devices to incorporate the above teachings of Vinal into the process of Ichimori et al. to maximize the carrier mobility and maximize the hot electron effects. See the abstract."

Applicant respectfully traverses the Section 103(a) rejection. Applicant submits that Vinal in view of Ichimori does not lend to a Gated-FET disclosed by the Applicant. Applicant also notes that the present rejection does not establish *prima facie* obviousness under 35 U.S.C. § 103 and M.P.E.P. §§ 2142-2143. The Examiner bears the initial burden to establish and support *prima facie* obviousness. *In re Rinehart*, 189 U.S.P.Q. 143 (CCPA 1976). To establish *prima facie* obviousness, three basic criteria must be met. M.P.E.P. § 2142.

> First, the Examiner must show some suggestion or motivation, either in the cited references or in the knowledge generally available to one of ordinary skill in the art, to modify the reference so as to produce the claimed invention. M.P.E.P. § 2143.01; *In re Fine*, 5 U.S.P.Q.2d 1596 (Fed. Cir. 1988). Second, the Examiner must establish that there is a reasonable expectation of success for the modification. M.P.E.P. § 2142. Third, the Examiner must establish that the prior art references teach or suggest all the claim limitations. M.P.E.P. §2143.03; *In re Royka*, 180 U.S.P.Q. 580 (CCPA 1974).
>
> Finally, the teachings, suggestions, and reasonable expectations of success must be found in the prior art, rather than in Applicant's disclosure. *In re Vaeck*, 20 U.S.P.Q.2d 1438 (CAFC 1991).

Applicant respectfully submits that a *prima facie* case of obviousness has not been met because the Examiner's rejection fails on all three of the above requirements.

(i) Lack of suggestion/motivation to combine & modify prior art to produce the claimed invention:

The examiner has ascertained that Ichimori has demonstrated: forming a substantially rectangular channel region in said semiconductor thin film layer, said channel region lightly doped to form a resistive channel, wherein the height of the channel region comprising the entire thin film thickness. The Applicant respectfully submit that Ichimori has not done so. The Applicant defines a channel and bulk regions as defined in page 13, lines 16-19 as listed below:

> "The term channel is used to identify a region that connects two other regions. The term body identifies a region common to a plurality of devices. The term body is also used to identify a substrate or a well region. The term body is also used to identify a region other than a conducting region."

Some may refer to Applicants channel region and/or bulk region as a channel region, without making the distinction between the two. Per this definition, in Ichimori Fig. 1, the region 16 is a "channel" region comprising the entire thin-film layer thickness if and only if the region 16 has the same dopant type as the two diffused regions 15 on either side. For example, if regions 15 are N+ doped, and region 16 is N doped, region 16 is a channel region. If region 16 is P doped when regions 15 are N+ doped, it is a bulk region. The latter case was shown as prior art in Applicants Fig-3. In the latter case, a minority carrier channel region is created by surface inversion of the underlying bulk region via a voltage applied to the gate. Ichimori calls the bulk region a channel region (para. 28, line 7) contrary to applicant's definition. Ichimori does not mention dopant types in the entire disclose; making a direct conclusion impossible. An inferred conclusion ascertains that region 16 is a bulk region. This is shown next. On para 21, lines 10, Ichimori states:

> "When the metal silicide layer (17) expands excessively into the diffusion layer (15) in the vertical direction or horizontal direction, the metal silicide layer becomes undesirable passage for current leakage at the channel region (16) under the gate electrode."

The applicant has added the parenthesis numbers pertaining to Fig-2A labels into Ichimori text above. There are two possible doping conditions between regions 15 & region 16.

(Case 1) If the regions 15 & 16 were both N type: There is no need for a diffused region 15 to be present, which would reduce process cost. The device would be a majority carrier device, and no source region is needed to supply minority carriers. Furthermore, if the silicide 17

encroached into region 16, there would be no leakage as the boundary between region 15 & 17 would be identical to a boundary between 16 & 17. This is contrary to Ichimori conclusion stated above. Ichimori indicates there is a leakage if the silicide gets too close to region 16, and he did use diffused regions 15 for his device. Both of these conditions suggest region 16 is not an N-type channel.

(Case 2) If region 16 was P type, while both regions 15 were N type: This is a minority carrier device, meaning, for conduction to occur the P type bulk region needs to be depleted, and a surface channel comprising N type minority carriers must be formed. There has to be an N type source attached to the inversion layer to supply these minority carriers – hence diffused N type regions 15 must be present. When silicide region 17 extends through region 15 and encroaches into region 16, there is a leakage current to bulk. Both these conditions are stated by Ichimori.

It is therefore concluded that Ichimori disclosure comprises a bulk region 16 formed between the diffused source/drain regions 15 under the gate. When a surface channel is created, it does not comprise of the entire thin-film thickness.

Vinal does not show: forming a substantially rectangular channel region in said semiconductor thin film layer, said channel region lightly doped to form a resistive channel, wherein the height of the channel region comprising the entire thin film thickness. The Applicant will also demonstrate that Vinal teaching cannot be applied to Ichimori due to the above & others limitations.

(1) First, the applicant will show that Vinal Fermi FET is a special embodiment of a four terminal depletion MOSFET as described by the Applicant prior art in Fig-1, discussed in page 4, line 15-21. Furthermore, the applicant will show that it is essential for depletion devices to have a channel region; and a bulk region below the channel region. Vinal, Fig-1A shows an N channel Fermi-FET (described in col 9, starting at line 48). Bulk 11 has acceptors (that is p-type dopant) N_a. Source/Drain regions 12/13 have heavy donors (that is n-type dopant) N_d^+. A bulk contact 22 is made at a diffused region 20 to bias the body 11 of the device (the fourth Bulk terminal of the device). A thin donor region (n-type) 15 doped N_d is formed adjacent to the gate region 14., beneath the gate electrode 23. The depth Y_0 of the region 15 is shown to be in the range 700A to 6000A (Table-1 in col 11). In col. 10, line 17, it is stated:

"The channel has depth Y_0 and a donor doping level N_d. The depth and doping and channel are critical for forming the Fermi-FET device of the present invention. In one embodiment, the substrate is a P-type substrate while source drain and channel regions are N-type."

The N doping profile in region 15 is carefully balanced against the P doping in the bulk region 16 to ensure that the carriers are depleted (see Eqs. 3A-3C, col. 10, lines 53-66). Without a P-type region under the N-type channel, there is no Fermi-FET. This is stated in col. 10, line 49 as follows:

"Given proper dose and depth, the implanted result of electron and hole diffusion across the junction between the channel 15 and the substrate 11. This carrier diffusion process is required to establish a constant Fermi potential across the P-N junction region."

To meet this design condition, full access to the bulk 16/11 potential via the contact 22 is required. This is described in col. 23, line 44. It is imperative that the Fermi-FET design comprises a channel region of opposite dopant to a bulk region. It is the careful arrangement of carrier distribution across the P-N junction that gives rise to the Fermi design concept.

(2) Second, the Applicant will show that in the Vinal SOI Fermi FET, the height of the channel region does not comprise the entire thin film thickness. Furthermore, the SOI Fermi-FET is also a four terminal device. In the previous section, we concluded that a P-N junction was essential for a Fermi-FET. This is seen in Vinal Fig-18, and described in col 35, line 57 - col. 36 line 25. In Fig-18, the thin-film region 44 has a thickness D, which is defined by Eq-78 in col.36. The source/drain regions are denoted 12/13 respectively. The channel region 15 has a depth A defined by Eq-77 in col. 36, which is less than the thickness D. Underneath the channel region 15, there is a bulk region 43 comprising a depth B. This depth B is stated in col. 36, line 14 to be the same value given by Eq-76 in col 35. Furthermore, the channel 15 is doped N-type, while the bulk 43 is doped P-type. As described in relation to Vinal Fermi FET earlier, the N-P doping balancing is the most critical design aspect of the Fermi FET. Clearly the channel 15 height is not the entire thin-film thickness. This structure is a special case of the Applicants Fig-3, shown as prior art, and described on page 6, line 13 through page 7 line 9. It is essential in Vinal Fermi-FET design to have a channel region AND a bulk region in the thin-film layer. There cannot be a single channel region comprising the entire thickness of the thin-film layer.

With reference to Vinal Figs. 23-26, the backplane (back substrate) 41 is shown to have contacts 22, and diffused regions 21. The reason is described in col. 37, lines 2 to be the same reason as for regular Fermi-FET. Furthermore, a voltage $-V_0$ is shown in Figs. 23-26 at the undepleted region of bulk region 43 and the oxide region 42 above the backplane region 41. This $-V_0$ voltage is established from the zero bias applied to backplane region 41, and would differ if not biased. Thus the Fermi condition is established by the potential applied at the bottom electrode 22, and maintained through the P-N regions with carrier dopant balancing. The absence of this fourth terminal would also violate the Fermi design.

(3) Third, the Applicant will show that Vinal SOI Fermi FET has a thin-film thickness requirement in complete disagreement with that defined by the Applicant. In Fig-18, the depth B of the remaining region 43 under the channel is described in col 36, line 14 to have the following property:

> "The depth B of the remaining channel substrate region 43 has the same requirements stated in Equation (76) for the SOI FET. That is, B must be sufficiently thick to ensure that channel substrate 43 is not completely depleted during carrier conduction when the drain is close to supply voltage Vdd."

From Fig-18, it is clearly seen that the SOI film 44 thickness D = A + B. The specifications for A & B can be obtained from Eq-77 & Eq-76 respectively to yield:

$D \geq [2e_s\phi_s/qN_a\alpha(1+\alpha)]^{1/2} + (2e_sV_{dd}/qN_a)^{1/2}$ -- (same as Eq-78)

[Please note that Eq-76 is incorrectly shown as $D \geq (2e_sV_{dd})^{1/2}/qN_a$; the correct expression is $D \geq (2e_sV_{dd}/qN_a)^{1/2}$]. In addition to the depth of channel A, the substrate depth B increases the SOI film thickness beyond the range described in the Applicant's film thickness. The Vinal SOI film thickness is specifically designed to be greater than the depletion width (B) as shown in Eq-78. In contrast, the Applicant describes a Gated FET device comprising a thin-film thickness that is less than the depletion width of majority carriers. This is discussed in the Applicant's application, page 24, line 7 to page 25, line 25, and defined by Equations 1-8. On page 24, line 7 the applicant specifies:

> "The channel 406 thickness T_S optimization to contain the fully depleted channel as discussed earlier is discussed in detail next. Two thickness parameters X and Y for a semiconductor material are defined by:
>
> $X = \varepsilon_S * T_G/\varepsilon_G$ Angstroms ----- (EQ 1)
>
> $Y = [(2*\varepsilon_S*V_{FB})/(q*D)]^{0.5}$ Angstroms ----- (EQ 2)
>
> $X_D = (X^2+Y^2)^{0.5} - X$ Angstroms ----- (EQ 3)

$T_S < X_D$ Angstroms ----- (EQ 4)

where, ε_S is channel semiconductor permittivity, ε_G is gate insulator permittivity, T_G is gate insulator thickness, V_{FB} is gate to semiconductor absolute flat band voltage, q is electron charge, D is channel doping level, X_D is the depletion depth and T_S is channel semiconductor layer thickness. EQ-3 denotes the maximum depletion width for the off Gated-FET shown as depth 641 in Fig-6A and depth 1041 in Fig-10A. The inequality in EQ-4 ensures film thicknesses 642 and 1042 shown Fig-6A and 10A respectively are within the maximum depletion depths 641 and 1041 into Silicon channel. Preferably T_S is chosen to be in the range $0.2*X_D$ to $0.9*X_D$, and more preferably T_S is chosen to be in the range $0.4*X_D$ to $0.8*X_D$ range."

Please note that Vinal D > B. For α=2 (ref. line 6, col. 18), ϕ_s=0.8V (ref. Eq-8E in col. 13 & line 31 in col. 15), V_{dd}=3V (ref. line 44, col. 35), A = 0.21B. So D ~ 1.2B (about 1.2x larger than B). Please note that the Applicant $T_s < X_D$. The thickness X_D in Applicant Eq-3 is smaller than the thickness Y by about 1.3x (shown in page 25, lines 1-5). Hence we can state that Applicants T_s < Y/1.3 = 0.77Y. Vinal Eq-76 (for parameter B) can be directly compared with Applicant Eq-2 (for parameter Y). Doping D in Applicant Eq-2 is same as doping N_a in Vinal Eq-76. These are assumed identical in both. Voltage V_{dd} in Vinal-76 is the power supply voltage, which can be 2.5V or 3.3V or 5.0V. In contrast, voltage V_{FB} in Applicant Eq-4 is the flat-band voltage, which is ~1V (ref. line 3, page 25). Thickness Y in Eq-2 is smaller than thickness B in Eq-76 by the ratio $(V_{dd}/V_{FB})^{0.5}$ - about 1.7x for V_{dd}=3V (ref. line 44, col. 35). The thin-film thickness requirements between Vinal and Applicant can be stated in common terms as:

$D_{VINAL} \geq 1.2*B$ $D_{APPLICANT} \leq 0.45*B$ (= 0.77*B/1.7)

The two requirements clearly do not overlap and contradict each other.

Neither Ichimori, nor Vinal has shown: forming a substantially rectangular channel region in said semiconductor thin film layer, said channel region lightly doped to form a resistive channel, wherein the height of the channel region comprising the entire thin film thickness. Further in view of the three additional conditions illustrated above for Vinal teaching, the Vinal SOI Fermi-FET could not be combined or modified in view of Ichimori to produce the Applicant's invention. Vinal must adhere to dual dopant regions between source & drain under the gate and provide a fourth electrode. Furthermore, Vinal SOI Fermi-FET design has a thin-film thickness specification contradictory to that of the Applicants Gated-FET design guidelines.

(ii) Lack of reasonable expectation of success for the modification:

Ichimori specifically describes a method of siliciding source/drain regions of an SOI device to improve junction leakage & reduce parasitic resistance. This is described in Ichimori para 20 – para 27. This is achieved as shown in Fig-2A/2B comprising three key elements: (1) a diffused region 15 is formed adjacent to the channel 16, the diffused region extending the full thickness of the thin-film layer, (2) a fully silicided region 17 is formed in the source/drain regions, the silicide extending the full thickness of the thin-film layer, and (3) a <111> silicide plane is achieved at the interface 18 (or 19) of the silicide region 17 and the diffused region 15, said salicided plane fully contained within the diffused region 15.

To prevent leakage and shorts, the structure shown in Fig-2A (or 2B) is carefully engineered as stated in para 22.

> "When the metal silicide layer expands excessively into the diffusion layer in the vertical direction or the horizontal direction, the metal silicide layer becomes an undesirable passage for current leakage at the channel region under the gate electrode. In fact, even if the metal silicide layers do not contact to the silicon substrate at the channel region, the leak pass is formed at the channel region when the metal silicide layers are formed closely enough. Therefore, it is necessary to form metal silicide layers to be smaller than the diffusion layers."

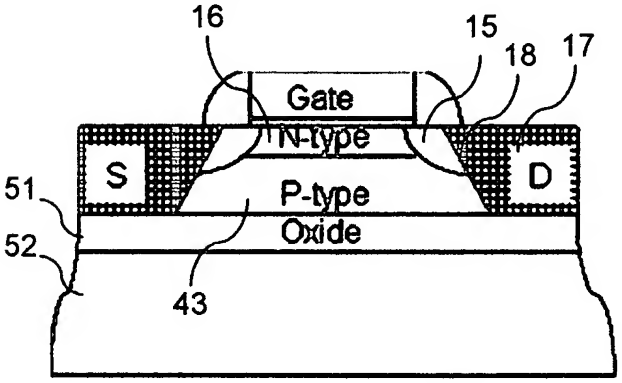

Fig-A: Hypothetical Vinal-Ichimori device

A hypothetical Vinal-Ichimori SOI device is constructed (Fig-A) by the Applicant to illustrate the discussion. The labels match Ichimori Fig-1 & 2. The region under the gate comprises of N-type channel 16 and P-type bulk 43. Per Ichimori, regions 17 are fully salicided all the way to the oxide 51 boundary. If the <111> silicide plane 18 crosses over into the channel region 16, there would be no problem. If the <111> silicide plane 18 touches the P-typr bulk region 43 as shown in Fig-A, the source & drain regions would short through to the bulk region. This would occur if there is no diffused junction 15, or if the diffused junction 15 did not fully

extend to the oxide layer 51 boundary (as shown in the diagram). To successfully adapt Vinal device in Ichimura process, it is critical that a diffused regions 15 is present, and that it extends to the bottom insulator 51 boundary, thereby preventing the <111> silicide interface 18 getting too close to P-type bulk region 43. This cannot be achieved as discussed below.

Three new events occur in a Vinal Fermi-FET in view of Ichimori. (1) Introduction of lightly doped drain regions in between the channel/drain regions, and associated thermal processing, (2) A new S/D silicide layer instead of doped regions, and associated thermal processing, and (3) Much deeper (1000A vs. 320A previous) penetration for diffused LDD regions, and Salicide regions, and associated thermal processing.

In para 31 & 37, Ichimura states that the silicon film thickness chosen is 320A. Vinal, col 35, line 41-48 states that for a doping level of 1E17 cm^{-3}, the silicon film thickness is 1000A (equivalently 0.1 microns). In col 36, line 27, Vinal also states a channel thickness as high as 6000A is needed for 4.3E16 cm^{-3} dopant in substrate. We will use 1000A for this analysis. If Vinal Fermi SOI FET was constructed in Ichimori process, the SOI film thickness in Fig-A would increase from the 320A to 1000A. The self aligned diffused regions 15 are introduced at the side wall (spacer) 14 processing step by implantation and then diffusion. This is a common LDD processing technique, also shown by Applicant in Fig. 14-5 (page 32, line 22). The LDD region formation requires a new thermal budget. The silicide process for S/D regions also requires a new thermal budget. The new thermal budget has to allow the junctions & silicide to penetrate to 1000A depth as compared to only 320A under Ichimori. Diffusion length has a $(\text{Diffusion coefficient} * \text{time})^{1/2}$ dependence on time. Hence a 10x longer time is required for this 3.2x deeper penetration to reach the full 1000A thickness. Ichimori para 33, line 3 states that 800C, 30 sec treatment is required for 320A silicide formation. The Vinal-Ichimori Fermi-FET would require at least 800C, 300 sec thermal treatment just for the silicde alone. In the SOI Fermi-FET, the N-type dopant profile in region 16 is carefully adjusted with the P-type substrate 43 dopant to yield the required depth. This is done prior to spacer, LDD and silicide formation. An 800C, 300 sec new thermal cycle would destroy the N-P dopant profile and the N-type region depth, thereby destroying the Fermi-FET design. The 6000A depth of thin-film layer would have been even more detrimental due to the increase in thermal budget.

Furthermore, the impact of adding an LDD region to the Vinal SOI Fermi-FET is an unknown factor. This would require an evaluation beyond the ordinary skill level of a person.

Thus a successful modification of Vinal in view of Ichimori is not possible due to the LDD regions, deeper LDD regions and thicker silicides needed. Ichimori scheme works best with thinner films, while Vinal scheme works better with thicker films.

(iii) Lack of prior art references to teach or suggest all the claim limitations (the teachings, suggestions, and reasonable expectations of success to be found in the prior art, rather than in Applicant's disclosure).

In section (i) above, the Applicant demonstrated that neither Ichimori, nor Vinal demonstrate:

> forming a substantially rectangular channel region in said semiconductor thin film layer, said channel region lightly doped to form a resistive channel, wherein the height of the channel region comprising the entire thin film thickness.

In section (i) above, the applicant also demonstrated that Vinal SOI Fermi-FET is a 4-terminal device that requires a substrate bias voltage. Vinal does not disclose operation of the device using only the single top gate without the substrate bias. Ichimori completely fails to disclose operation of the device. Neither Ichimori, nor Vinal demonstrate:

> a first (gate) voltage level that modulates said channel resistance to a substantially non-conductive state by fully depleting majority carriers from said channel region; and
>
> a second (gate) voltage level that modulates said channel resistance to a substantially conductive state by at least partially accumulating majority carriers near the gate insulator surface in said channel region.

For a successful adaptation of Vinal in view of Ichimori, there needs to be a suggestion or a motivation in either of the reference disclosures to construct a three terminal, single dopant resistive channel thin-film device. The examiner has mentioned the motivation factors to be: (i) maximize carrier mobility, and (ii) minimize the hot electrons as stated by Vinal. Both these conditions are achieved by Vinal from minimizing the vertical electric field (col. 4, line 66 – col. 5, line 5). To do so, as per Vinal, N-P doped regions are required in the device between the source and drain regions (col. 5, lines 15-20), and a controlled back-plane potential is also needed to achieve this (col. 23 line 44 to col. 24, line 28). Both these conditions are de-

motivating reasons to design a three terminal, single dopant resistive channel device as described by the Applicant. Ichimori device already comprises LDD (lightly doped drain regions 15 in Fig-1), which also reduces hot electrons. Ichimori must have these diffusion regions, as discussed by the Applicant previously. Vinal does not use LDD diffusions, instead opting for regular highly doped drains (N++ regions 12/13 in Fig-10A). Clearly Vinal would benefits from reduced hot electrons in Fermi-FET design. However, a reader skilled in the art would not be motivated to adapt Vinal Fermi-FET to an existing LDD process of Ichimori for the sake of hot electron reduction.

> In order to be unpatentable, 35 U.S.C. 103(a) requires that an invention must have been obvious to a person having "ordinary skill in the art" to which the subject matter sought to be patented pertains. The "level of ordinary skill in the art" from which obviousness of a design claim must be evaluated under 35 U.S.C. 103(a) has been held by the courts to be the perspective of the "designer of . . . articles of the types presented." In re Nalbandian, 661 F.2d 1214, 1216, 211 USPQ 782, 784 (CCPA 1981); In re Carter, 673 F.2d 1378, 213 USPQ 625 (CCPA 1982).

The rationale to modify or combine the prior art to construct a Gated FET is not expressly or impliedly stated in the prior art in Ichimori & Vinal. As all of the three conditions for a *prima facie* case of obviousness have not been met, it would not be obvious to one with ordinary skill to arrive at the Applicants disclosures stated in the independent claims 1, 13 and 17. Hence Applicant's independent claims 1, 13 & 17 would have not been obvious under Vinal in view of Ichimura. Withdrawal of the rejections of independent Claims 1, 13 & 17, and those dependent thereupon is respectfully requested.

3.1.2 Claim-5 rejection:

The examiner noted that:

> "Houston teaches choosing high work function material for the gate region when the device is p channel or p doped channel and low work function material for the gate region when the device is n channel or n doped channel to provide higher threshold voltage. See [0023]."

Houston discloses a DRAM memory device that integrates an SOI thin-film pass gate device with SOI thin-film peripheral devices. The gate material work function is used to increase the threshold for the pass-gate device, without the need to increase channel doping. Houston also shows SOI MOSFET devices as discussed by the Applicant in Fig-3. This is seen with respect to

Houston Fig-5 and Fig-6. For example, if device 45 in Fig-6 has a single dopant resistive channel under the gate comprising the full thickness of the thin-film layer, device 45 would short to device 46. However, if device 45 has a bulk region under the gate, the two devices 45 & 46 can co-exist side by side as shown. (In MOSFET design, the P-well is common to all NMOS devices, and the N-well is common to all PMOS devices). Hence Houston devices must comprise both a channel region (either by surface inversion during conduction similar to MOSFET, or created by a thin implanted region similar to Vinal) and a bulk region (underneath the channel). For isolation purposes, N-channel devices reside in P-type bulk regions (P wells), and P-channel devices reside in N-type bulk regions (N wells).

As Houston in view of Ichimori does not teach forming a single dopant channel region, wherein the height of the channel region comprising the entire thin film thickness, withdrawal of the rejection is respectfully requested.

3.1.2 Claim-6 rejection:

The examiner noted that:

> "Further with respect to claim 6, a conducting path comprising the entire thickness of the thin film layer would inherently be formed between the source and drain and through the channel region in the process of Ichimori et al."

An SOI MOSFET shown by the Applicant in Fig-3 is same as the Ichimori device. On page 6, line 13, the Applicant has demonstrated that such a device has a bulk region coupling the source and drain regions. During conduction, a surface channel region 310 is formed, as shown in Fig-3A. This very shallow channel height does not comprise the entire thin-film thickness. The Applicant has presented arguments to demonstrate that Ichimori device is similar to that shown in Fig-3 by the Applicant (please see the previous sections). Withdrawal of the rejection is respectfully requested.

4. Allowable Subject Matter:

In section 4, The examiner noted that

> "Claims 7-12 and 14-16 and 18-20 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims."

The Applicant has herewith presented arguments as to why independent Claim-1, 13 and 17 are distinctly different from Vinal in view of Ichimori sighted in this office action. Withdrawal of those rejections was requested, and if granted, would absolve the objection listed above. Withdrawal of all objections by the examiner, in view of the requested withdrawal of prior rejections, is respectfully requested.

In summary, the Applicant submits that all claims as presented in this response are allowable in view of the Vinal further in view of Ichimori, and claim 5 is allowable in view of Houston further in view of Ichimori. Withdrawal of all objections and rejections is respectfully requested.

CONCLUSION

The applicant believes that the above submission is fully responsive to the office action.

If for any reason the Examiner believes that a telephone conference would in any way expedite this matter, the Examiner is invited to telephone the Inventor Mr. Madurawe at (408) 737-8868 or on his cell phone at (408) 431-5367.

Respectfully submitted,

Raminda Madurawe

Raminda Madurawe